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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,465	06/30/2003	Sau Ching Wong	MLM003US1D	1603

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PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,465	WONG, SAU CHING	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/30/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Preliminary Amendment

1. Acknowledgment is made of applicant's Preliminary Amendment, filed 30 June 2003. The changes and remarks disclosed therein were considered.

Claims 1-11, 25 and 26 have been cancelled. Therefore, claims 12-24 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 30 June 2003. The information disclosed therein was considered.

Specification

3. The disclosure is objected to because of the following informalities:

In the first paragraph, the status of the parent application should be updated. Namely, the parent application U.S. Pat. App. No. 09/927,693 has now matured into U.S. Pat. No. 6,614,685.

Appropriate correction is required.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 12-15 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (U.S. Pat. No. 5,835,436) in view of Hazen et al. (U.S. Pat. No. 6,088,264).

Regarding claims 12 and 18, Ooishi, for example in Figs. 30, 32 and 64 (as applied to the alternative for repairing defective array blocks, disclosed in column 63, lines 48-67), discloses a memory, and a related operating method, comprising: memory elements having respective physical addresses that correspond to logical addresses of the memory ("normal array blocks" or "general array blocks" in column 63, lines 48-67); spare memory elements having respective physical address that do not correspond to the logical addresses of the memory ("array block for substitution" or "additional array block" or "spare array block" in column 63, lines 48-67); a content addressable memory array (within 202 in Figs. 30 and 32, or 1610 in Fig. 64) coupled to receive a logical address signal (or a first logical address) (INPUT ADDRESS A1-A8 in Fig. 64, for block selection, since the repair is at the block level) from an external device (see for

example column 65, lines 30-32) for comparison with defect addresses (ENT1 - ENTn in Fig. 32) stored in the content addressable memory array; a memory array (REG1 - REGn in Fig. 32) having word lines (within 204 in Fig. 32) coupled to respective match lines (CHL1 - CHLn in Fig. 32) of the content addressable memory array, wherein in response to activation of one of the match lines, the memory array outputs a substitute address signal (the output of 204 or 1612) representing a substitute address stored in a row (of 204 in Fig. 32) corresponding to the activated match line (see Fig. 32); and multiplexing circuitry (206 or 1616) connected to select between the logical address signal (via 200 or 1614) and the substitute address signal as a physical address signal (INTERNAL ADDRESS in Fig. 64), the multiplexing circuitry providing the physical address signal for selection of a memory cell being accessed.

However, Ooishi does not disclose that the memory is a Flash memory.

Hazen disclose a Flash memory with a plurality of blocks (see for example column 2, lines 23-43).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the repair means of Ooishi (including spare blocks and an address conversion circuit) in the Hazen's Flash memory with blocks, for the purpose of providing an efficient repair capability in Flash memories with blocks and therefore increasing the manufacturing yield of such memories.

Regarding claims 13-15 and 22-24, the above Ooishi/Hazen combination further discloses that each memory element and each spare memory element is a block of memory cells that are connected to permit simultaneous erasure of all of the memory cells in the block (see for

example column 2, lines 39-41 of Hazen); that the memory further comprises a write data path (inherent) and a read data path (inherent), wherein the blocks are organized into a plurality of array planes (for example, "partitions" A, B, C, etc. in column 2, lines 23-43 and Fig. 2 of Hazen), the array planes being connected to the write and read data path so as to permit any one of the array planes to conduct a read operation while any other of the array planes conducts a write operation (see for example column 2, lines 23-43 of Hazen); that each array plane contains erase circuit that permits the array plane to erase a block in the array plane, while other array planes conduct read and write operations (see column 2, lines 23-43 of Hazen).

Regarding claims 19-21, the above Ooishi/Hazen combination further discloses applying a second logical address (for example, a row address; see claim 13 of Ooishi) from the external device directly to a decoder (a row address decoder) in the memory while applying the first logical address to the content addressable memory, wherein a combination of the first and second logical addresses identifies a memory cell (along with a column address); wherein the first logical address is a block address (since, in Ooishi, the repair is at the block level) and the second logical address identifies a memory cell within a block (along with a column address); wherein the second logical address is a row address (see for example claim 13 of Ooishi).

7. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (U.S. Pat. No. 5,835,436) in view of Hazen et al. (U.S. Pat. No. 6,088,264) as applied to claim 14 above, and further in view of Hidaka (U.S. Pat. No. 6,233,181) and Abedifard et al. (U.S. Pat. No. 6,665,221).

The above Ooishi/Hazen combination discloses a memory as in claim 14, with the exception of each array plane comprising at least one of the spare memory elements and a spare global bit line that connects to all blocks in the array plane.

Hidaka discloses array planes (for example, "row blocks" RB#m in Fig. 1), each comprising at least one spare memory element (for example, SPARE ARRAY SP#m) and a spare global bit line (SGIO).

Abedifard, for example in Fig. 5, discloses a spare global bit line (420 in the redundant column 428) that connects to all blocks (MB0-MB3) in an array plane.

Since, in Hazen, each array plane (or partition) with blocks is disclosed as an operational unit (i.e., when two or more planes are simultaneously accessed, each plane of blocks, as a unit, has a designated access operation, such as read, write or erase), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate at least one spare memory element (or block) and a spare global bit line in each array plane (or partition) of the Ooishi/Hazen combination, as in Hidaka, for the purpose of providing additional levels of redundancy and repair capability and therefore further increasing the yield of such memories.

Further, since grouping of blocks in a column direction within a plane or partition (such that global bit lines and spare global bit lines, if any, connects to all the blocks) is an obvious variation of the Hidaka's grouping of blocks in a row direction and is common and well known in the art, as exemplified by Abedifard, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to group the blocks, including the spare block, in a column direction within the array planes of the Ooishi/Hazen combination, such that a spare global bit line connects to all the blocks in the array plane, for the purpose of providing

additional levels of redundancy and repair capability and therefore further increasing the yield of such memories.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Jungroth et al. (U.S. Pat. No. 5,621,690) discloses a flash memory with a block redundancy.

Brennan, Jr. (U.S. Pat. No. 5,233,559) discloses a flash memory with a row redundancy.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

VAN THU NGUYEN
PRIMARY EXAMINER